IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner: Hong Kim
Serial No.:	08/984,563	Group Art Unit: 2185
Filed:	December 3, 1997	Docket: 303.623US4
Title:	ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION	

REPLY BRIEF UNDER 37 CFR § 41.41

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Reply Brief is presented in response to the Examiner's Answer, dated July 16, 2007, which was sent as a reply to Appellants' Appeal Brief, filed on January 25, 2007. Appellants' Appeal Brief was filed in response to the rejection of claims 59-62 and 68-69 in the above-identified Application, as set forth in the Final Office Action dated August 30, 2006 ("Final Office Action"). Please charge any required additional fees or credit overpayments to Deposit Account 19-0743.

REMARKS

The Examiner's Answer Brief, ("Examiner's Answer") dated July 16, 2007, includes substantially identical grounds for rejection as the Final Office Action. Appellant respectfully maintains that the Appeal Brief, which is hereby incorporated by reference and reasserted in response, overcomes the original grounds of rejections.

Status of the Claims

The Appellants confirm that the current status of the claims is as follows: claims 36-39, 63-67 and 75-83 have been allowed; claims 70-74 were previously canceled; and claims 59-62 and 68-69 stand rejected under 35 U.S.C. § 103(a).

Response by Appellants to General Arguments in the Answer

There are two fundamental principles that should be kept in mind when considering the detailed response to various arguments in the Answer that are asserted in the following section: the difference between a pipelined architecture and a pipelined mode of operation; and the fact that the Office has approved language from the Appellants, in a related matter, to the effect that Manning fails to disclose switching between burst and pipelined modes. These principles are explained in detail hereinbelow.

Difference Between The Pipelined Mode Claimed by Appellants And a Pipelined Architecture: It should be noted that a pipelined architecture does not equal the pipelined mode claimed by Appellants. As noted in the Appeal Brief filed by Appellants in a related matter (Application Ser. No. 08/984,701), another way of viewing whether they are the same is to ask the question: how can a memory have a pipelined architecture (as mentioned by Manning) without inherently operating in the pipelined mode claimed by the Appellants? The brief answer is that a memory, such as a burst EDO memory, may include pipelined registers that permit the rapid generation of internal addresses. However, external addresses are still received and processed in the same fashion as regular EDO memory.

Burst EDO memory improves EDO performance by adding a pipeline stage (i.e. a pipelined architecture) to permit reads or writes to occur in four row-address bursts. After the initial page address is applied to a burst EDO chip, the chip typically provides three more

sequential addresses (within a page). This address circuitry eliminates the time required to detect and latch externally supplied addresses. However, burst EDO memory including a pipelined architecture *does not accept external addresses so as to operate in a pipelined mode* (as defined by the Appellants in the Application).

A true pipelined mode of operation makes use of time slicing address information so that external accesses to a memory may overlap internal operations without conflicting. This allows for a continuous data stream of address information in the form of external addresses. Thus, *internal addresses are not generated in pipelined mode.* Rather, addresses are provided from an external source as a stream of data.

The Office Approves Appellants' Language Stating That Manning Does Not Teach Selecting/Switching Between Burst Mode And Pipelined Mode: As stated by the Board of Patent Appeals and interferences (BPAI) in a related matter (Application Ser. No. 08/984,562), "Manning provides no details as to how the use of a pipelined structure might be accomplished. We agree with appellants. Manning's suggestion to use a pipeline architecture is insufficient to suggest switching between burst and pipelined modes. As indicated *supra*, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur. Accordingly, we cannot sustain the obviousness rejection ...". BPAI, Appeal No. 2005-1725, March. 20, 2006. Thus, the BPAI approves Appellants' language stating that Manning fails to teach switching between burst and pipelined modes.

Response by the Appellants to Specific Arguments in the Answer

Specific references to claims in the Answer have been separated into the following groups corresponding to distinct arguments offered by the Office, rather than using any particular grouping that might be applied to the claims with respect to considerations of independence and/or patentability. Thus, the groups below have been created to provide convenient review of the Appellants' response to recurring arguments in the Answer, and not as a means of grouping the claims for consideration by the Board on less than an individual basis. The response for each group will be presented in the form of a statement in the Answer, and a factual correction in the response.

Group I (Independent claims 59 and 68-69):

Statement -- Manning further teaches claimed limitation of choosing between a burst or a pipeline mode operation.

Response -- The Answer quotes "switching between fast page mode, EDO page mode, static column mode and burst operation (Manning, col. 7, lines 40-55)", and then goes on to assert that "since the **pipelined architecture** can be used on the fast page mode, EDO page mode, static column mode and burst operation in order to increase accessing speed and switching between the various modes is possible..." (emphasis added). The Office then concludes that "Manning further teaches claimed limitation of choosing between a burst or **a pipeline mode** of operation" (emphasis added). Appellants disagree, and respectfully argue that the conditions set forth by the Office are insufficient to reach this conclusion, because as noted above, there are differences between a **pipelined architecture** and the **pipelined mode** claimed by Appellants.

As admitted in the Answer, "Manning does not specifically disclose detailed operation of a pipeline mode." As noted above, the BPAI approves Appellants' language stating that Manning fails to teach switching between burst and pipelined modes. See BPAI, Appeal No. 2005-1725, March. 20, 2006, page 6. Thus, the statement in the Answer that Manning further teaches the claimed limitation of choosing between a burst or a pipeline mode operation contradicts the above approval by the BPAI. Therefore, Manning does not teach selecting/switching between a burst and pipeline mode.

Group II (Independent claims 59 and 68-69):

Statement -- Roy discloses the memory selectively operable in a pipeline mode.

Response -- The interpretation by the Office of a "pipelined mode" with respect to Roy is improper. Roy describes a memory device capable of column burst activity where sequential bytes of data are accessed using a starting column and row address and a burst length. *See* Roy, Col. 26, lines 62-66. New actions may be initiated when a burst is completed. *See Id.* at Col. 27, lines 4-14. The device may also be used in a pseudo-pipelined access mode, such that a new column address is provided every cycle for a random read operation, as long as it is confined to a selected row. *See Id.* at Col. 28, lines 16-32 and Col. 33, lines 8-19. While limited access

pseudo-pipelined reads may occur once per cycle, pseudo-pipelined write operations occur at only one-half the maximum channel frequency, since channel access is shared by both addresses and data. *See Id.* at Col. 33, lines 65-67. This is in direct contrast to the teachings of the Applicant, which enable true pipelined operation, with column-based switching in addition to row-based switching (See Application, pg. 38, lines 7-16). The Applicant was unable to find any indication that Roy enables selecting true pipelined and burst operation "on the fly" as demonstrated by the Applicant's disclosed embodiments. Indeed, Roy imposes operational restrictions due to software header mode changes and channel data/address sharing. For example, Roy does not permit row-based switching operation (i.e., "... cannot be used to change a row in every cycle ..."). *Id.* at Col. 38, lines 23-24.

Thus, the interpretation of the term "pipelined mode" proffered by the Office with respect to Roy is neither reasonable, nor consistent with the specification. It is not reasonable because it contradicts the meaning of the term as understood by those of skill in the art. The interpretation by the Office is also not consistent with the specification. Thus, any attempt by the Office to characterize Roy as teaching a true "pipelined mode" of operation is beyond that which should be reasonably allowed. Therefore, Roy does not disclose the "pipeline mode" as recited in the rejected claims.

Group III (Independent claims 59 and 68-69):

Statement -- Ogawa discloses the memory selectively operable in a pipeline mode.

Response -- Ogawa does not teach any kind of switching behavior. Pipelined access of Ogawa is described solely with respect to a single mode of operation – the page mode. *See* Ogawa, Abstract and Col. 1, lines 8-12. "The page mode processing is an operation that subsequently reads out data in memory cells connected to one word line selected by a row address by sequentially changing the column address ...". Col. 4, lines 4-8. While Ogawa notes that "the present invention is not limited to the page mode, and the concept of the present invention can be similarly applied to random read/write operation" at Col. Col. 12, lines 5-10, this statement of potential use with respect to random read/write operations does not lead one of ordinary skill to understand how switching between burst and pipelined modes would be accomplished, since Ogawa does not teach any kind of switching behavior. As such, Ogawa

provides no indication of how memory access operations can be conducted in conjunction with switching between burst an pipelined modes "on the fly" as taught by the Appellant.

In sum, quoting the BPAI, "As indicated **supra**, we find nothing in Manning to suggest substituting a pipelined mode for the standard EDO such that selecting or switching between burst and pipelined modes can occur." BPAI, Appeal No. 2005-1725, March. 20, 2006 (emphasis in original). In addition, Roy does not disclose the "pipeline mode" as recited in the rejected claims. Finally, Ogawa does not teach any kind of switching behavior. The Appellant finds nothing in Manning to suggest substituting a pipelined mode for the page mode, as promoted by the Office with respect to Ogawa. Therefore, no combination of Manning and either Roy or Ogawa can provide "choosing whether the memory is in a burst mode of operation or a pipelined mode of operation" (claim 59) or "selecting a burst or a pipeline mode of operation" (claim 68), much less "mode circuitry configured to select between a burst mode and a pipelined mode" (claim 69) as claimed by the Appellant.

Other statements of alleged fact, unsupported by any reference, are presented in the Answer. A few of these statements are quoted below:

(a) "... it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input, or memory data output to be processed simultaneously";

(b) "the pipelined architecture requires only a single sample-and-hold circuit per read or write circuit"; and

(c) "the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area".

Even if these statements were supported by evidence, they do nothing to remedy the deficiency of Manning. There is simply no reference to a true pipelined mode of operation within the bounds of Manning, as explained at length in the Appeal Brief. Thus, the assertion that Manning teaches a pipelined mode of operation is simply not supported by the evidence in the record.

Conclusion

Appellants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone the Appellants' attorney at (210) 308-5677 to facilitate prosecution of this Application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(210) 308-5677

Date: September 14, 2007 By /Mark V. Muller/
Mark V Muller
Reg. No. 37,509

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14th day of September, 2007.

Amy Moriarty
Name

Signature